

### Abstract of Disclose

A self refresh operation control device, for use in a semiconductor memory device, includes a self refresh pulse  
5 signal generation block for generating a self refresh pulse  
signal, a self refresh entry signal and a self refresh mode  
clock enable signal in response to a clock enable signal, a  
self refresh signal, a self refresh end signal and a test mode  
signal, wherein the self refresh pulse signal is generated  
10 during the inactivated period of the clock enable signal by  
using the test mode signal; a normal mode clock signal  
generation block for generating a normal mode clock signal and  
a counter reset signal in response to the clock enable signal,  
the self refresh mode clock enable signal, a test mode signal  
15 and the self refresh signal; and an internal row address  
counter in response to the self refresh pulse signal and the  
counter reset signal for generating internal addresses for use  
in the self refresh operation.